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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

OIPE JC177 APR 2 5 2001 PATENT & TRADEMARK OFFICE

In re Patent Application of

LILLINGTON

Serial No. 09/774,673

Filed: February 1, 2001

For: FREQUENCY ANALYSIS

Atty. Ref.: 550-204

Group: 2631

Examiner:

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April 25, 2001

Assistant Commissioner for Patents
Washington, DC 20231

SUBMISSION OF PRIORITY DOCUMENTS

Sir:

It is respectfully requested that this application be given the benefit of the foreign filing date under the provisions of 35 U.S.C. §119 of the following, a certified copy of which is submitted herewith:

Application No.	Country of Origin	Filed
0004700.1	UK	28 February 2000

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: ______________________

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Dated 26 January 2001

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29FEB00 E517009-5 002246
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1.	**Your reference**	P008543GB
2.	**Patent application number** *(The Patent Office will fill in this part)*	28 FEB 2000 **0004700.1**
3.	**Full name, address and postcode of the or of each applicant** *(underline all surnames)*	John Lillington Seymour House 19 Nodgham Lane Carisbrooke Isle of Wight PO30 1NY
	Patents ADP number *(if you know it)*	5935705002
	If the applicant is a corporate body, give the country/state of its incorporation	United Kingdom
4.	**Title of the invention**	Frequency Analysis
5.	**Name of your agent** *(if you have one)*	D YOUNG & CO
	"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	21 NEW FETTER LANE LONDON EC4A 1DA
	Patents ADP number *(if you have one)*	59006

6. **If you are declaring priority from one or more earlier patent applications, give the country and date of filing of the or each of these earlier applications and (if you know it) the or each application number**

Country	Priority application number *(if you know it)*	Date of filing *(day/month/year)*

7. **If this application is divided or otherwise derived from an earlier UK application, give the number and filing date of the earlier application**

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8. **Is a statement of inventorship and of right to grant of a patent required in support of this request?** *(Answer 'Yes' if:*
a) any applicant named in part 3 is not an inventor, or
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Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	0
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Any other documents *(please specify)*	No

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11. **I/We request the grant of a patent on the basis of this application.**

Signature D Young & Co.

D YOUNG & CO
Agents for the Applicants

Date 28 Feb 2000

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12. **Name and daytime telephone number of the person to contact in the United Kingdom**

N A J Robinson 023 8063 4816

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FREQUENCY ANALYSIS

This invention relates to digital signal processing (DSP) techniques for analysing the frequency content of a signal.

The most common known method employed to perform frequency analysis is the FFT (Fast Fourier Transform) method which has embodiments in both software algorithms and in hardware form. The FFT approach suffers from the disadvantage that it is better suited to software implementations rather than programmable hardware.

Viewed from one aspect the invention provides apparatus for frequency content analysing an input signal, said apparatus comprising a plurality of frequency splitting stages, each stage including one or more up-converter and down-converter pairs, an up-converter and down-converter pair serving to receive a complex input signal representing an input bandwidth and to output a first complex output signal representing an upper portion of said input bandwidth and a second complex output signal representing a lower portion of said input bandwidth, said first portion and said second portion being contiguous and together representing said input bandwidth portion.

In one form, the invention may be embodied as a "tree" system by successively splitting the frequency band of interest into two separate contiguous bands, each one being centred on zero frequency (zero IF). This is achieved by using complex up and down-converters. However, for resolution into a useful number of bands, a large number of complex converters is required (e.g for 1024 bands, we would need 2047 converters). This is a disadvantage.

In order to allow the same result to be achieved with far fewer converters, preferred embodiments of the invention interleave the samples from the upper and lower portion at each stage and passing them through a modified form of up / down-converter in the next stage. In general, this requires only $1+2*\mathrm{Log}_2$ (N) stages where N equals the final number of frequency bands. For example, 1024 bands would now

require only 11 converters, compared with the 2047 mentioned above for the "tree" system above.

This technique is practicable and has a similar economy of scale as the FFT has over the more direct DFT (Discrete Fourier Transform) methods.

The invention may also be viewed as a corresponding method of frequency content analysis.

Example embodiments of the invention are described below.

Figure 2.1 below gives a simplified block diagram of a 3 stage tree system. The input to the system is a band limited signal, centred on zero frequency (or zero IF). The sample rate is F_s and, by using a complex (I&Q) form, the input band can occupy from $F_s/2$ to $+ F_s/2$, as illustrated in Figure 2.2. The input is now split into two bands by using a Complex Down-Converter (CDC) and a Complex Up-Converter (CUC). Thus, in Figure 2.2, the *upper* half of the input band (i.e. 0 to $+ F_s/2$) is down-converted to the band $-F_s/4$ to $+F_s/4$. Similarly, the *lower* half of the input band is up-converted to the band $-F_s/4$ to $+F_s/4$.

The realisation of the complex down-converter (CDC) is shown in Figure 2.3 and the complex up-converter (CUC) in Figure 2.4 These are intended to show the principle of operation only. The actual realisation can be much simplified since the Sine and Cosine need only take one of five values (0, +1, -1, +0.707 and –0.707).

The overall block diagram is shown in Figure 3.1. The first pair of converters (CDC 'A' and CUC 'A') are identical with those of the "tree" system (Fig. 2.1). Thereafter, however, the samples for the 'I' channel and for the 'Q' channel are interleaved before passing to the next stage of processing.

The Interleaved Complex Down-Converter (ICDC) differs from the CDC of the "tree" system in that the Low Pass Filters are now of a special form, typically

known as "Interpolating FIR Filters". By adding additional delay between the taps of a FIR (Finite Impulse Response) filter, it is possible to process any number of independent data streams by first interleaving them. The filtered output data is also interleaved in the same manner. The requirements are that each of the independent data streams needs to processed by an *identical* filter and that the Interpolating FIR filter is capable of running at the increased sample rate caused by interleaving the input data. Since each of the CDC's of the "Tree" system in any one filter bank are identical, the first requirement is met. Also, although the number of independent sample streams increases by a factor of two at each branch of the tree, the sample rate also drops by a factor of two. Thus it is possible to interleave the samples without any overall increase in sample rate, thus satisfying the second requirement above.

Exactly the same arguments apply to the Interleaved Complex Up-Converter (ICUC). The final output of the interleaved system is identical with that of the "Tree" system except that, of course, the "Tree" system outputs are in parallel form whereas the "Interleaved" system outputs are in serial form.

Further details of the interleaving and decimation process are as follows. Referring to Figs.3.1 and 3.2, the complex stream of input samples to CDC(A) and CUC(A) are designated I_1, I_2, I_3,.....etc. and Q_1, Q_2, Q_3,.....etc. at a sample rate of F_s. The output of the Complex Down-Converter (CDC(A)) is the filtered sample stream, designated I_{d1}, I_{d2}, I_{d3},.....etc. and Q_{d1}, Q_{d2}, Q_{d3},.....etc. and the corresponding output from the Complex Up-Converter (CUC(A)) is the filtered sample stream, designated I_{u1}, I_{u2}, I_{u3},.....etc. and Q_{u1}, Q_{u2}, Q_{u3},.....etc. These output sample streams are also at a sample rate of F_s.

A pair of simple interleavers then follow which interleave the I samples, giving the stream I_{d1}, I_{u2}, I_{d2}, I_{u2}, I_{d3}, I_{u3} ...etc. and also the Q samples giving the stream Q_{d1}, Q_{u2}, Q_{d2}, Q_{u2}, Q_{d3}, Q_{u3} ... etc. These are now at the increased sample rate of $2F_s$.

The interleaved I and Q sample streams are then processed by the Interleaved Complex Up and Down-Converters (ICDC(B) and ICUC(B)). The complex output data stream from ICDC(B) is designated I_{dd1} , I_{ud2} , I_{dd2} , I_{ud2} , I_{dd3} , I_{ud3} ,.... Etc. and Q_{dd1} , Q_{ud2} , Q_{dd2} , Q_{ud2} , Q_{dd3} , Q_{ud3} ,.... Etc. The complex output data stream from ICUC(B) is designated I_{dd1} , I_{ud2} , I_{dd2} , I_{ud2} , I_{dd3} , I_{ud3} ,.... Etc. and Q_{dd1} , Q_{ud2} , Q_{dd2} , Q_{ud2} , Q_{dd3} , Q_{ud3} ,.... Etc. The sample rate at this point is still $2F_s$ which is twice the necessary rate. It is not possible, however, to simply decimate the samples by a factor of two (i.e. to remove every other sample) because of the interleaved nature of the samples. Instead, it is necessary to accept the first and second sample of each stream, remove the third and fourth, accept the fifth and sixth sample and so on before interleaving. This yields sample streams at the output of the 2:4 Complex Interleaver / Decimator as follows :-

I_{dd1} , I_{du1} , I_{ud1} , I_{uu1} , I_{dd3} , I_{du3} ,.... Etc. and Q_{dd1} , Q_{ud2} , Q_{dd2} , Q_{ud2} , Q_{dd3} , Q_{ud3} ,.... Etc.

For any subsequent stages, the interleaver / decimator principle is the same. For example, the following stage would retain samples 1,2,3 and 4, discard samples 5,6,7and 8, remove samples 9,10,11and 12 (etc.) before interleaving. The next stage would retain samples 1 through 8, discard samples 9 through 16 and so on. The implementation of this process can be carried out in various ways including, for example, switched FIFO (first in first out) memory with the read rate set to half the write rate

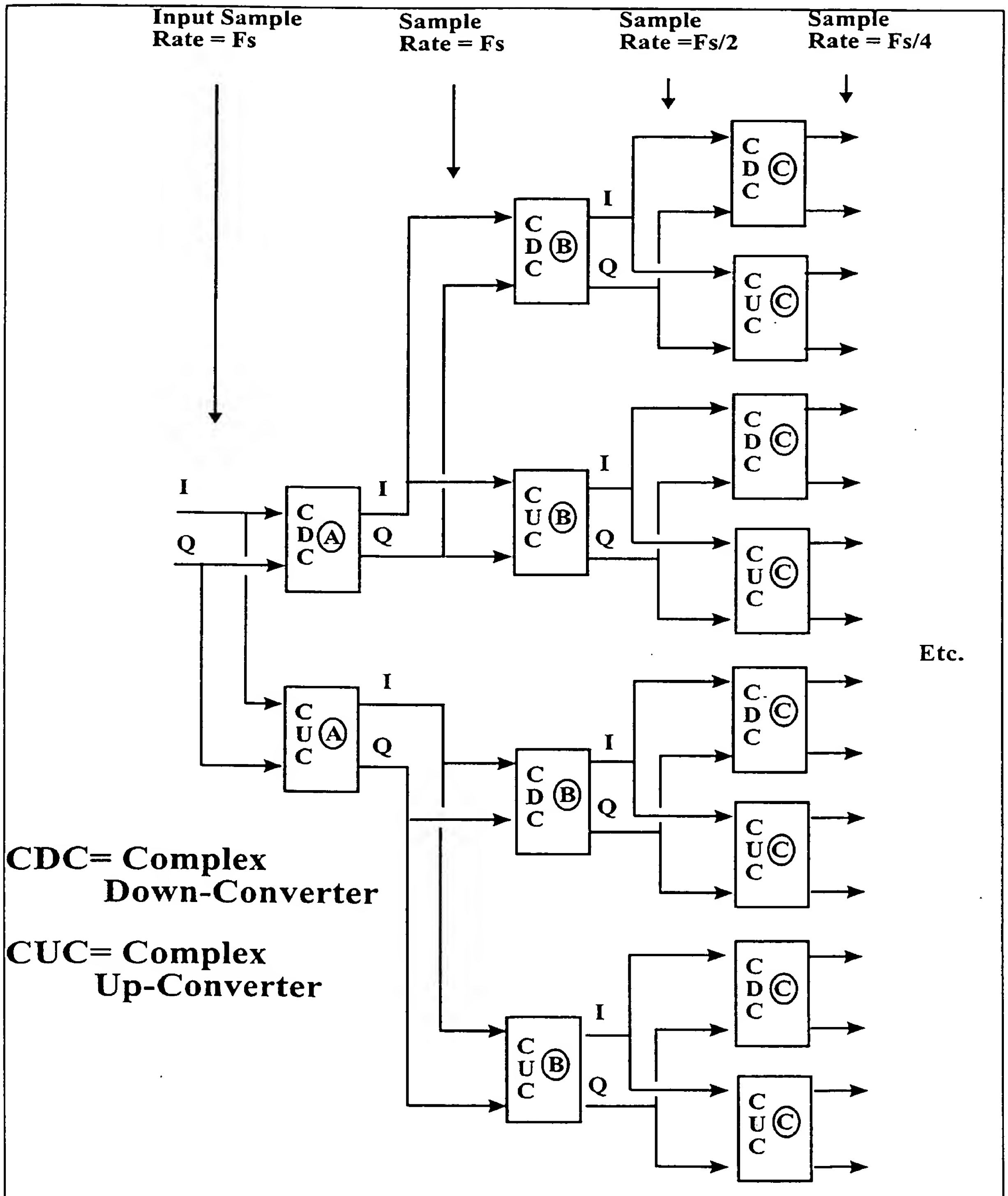

Fig. 2.1 Block Diagram of Tree System

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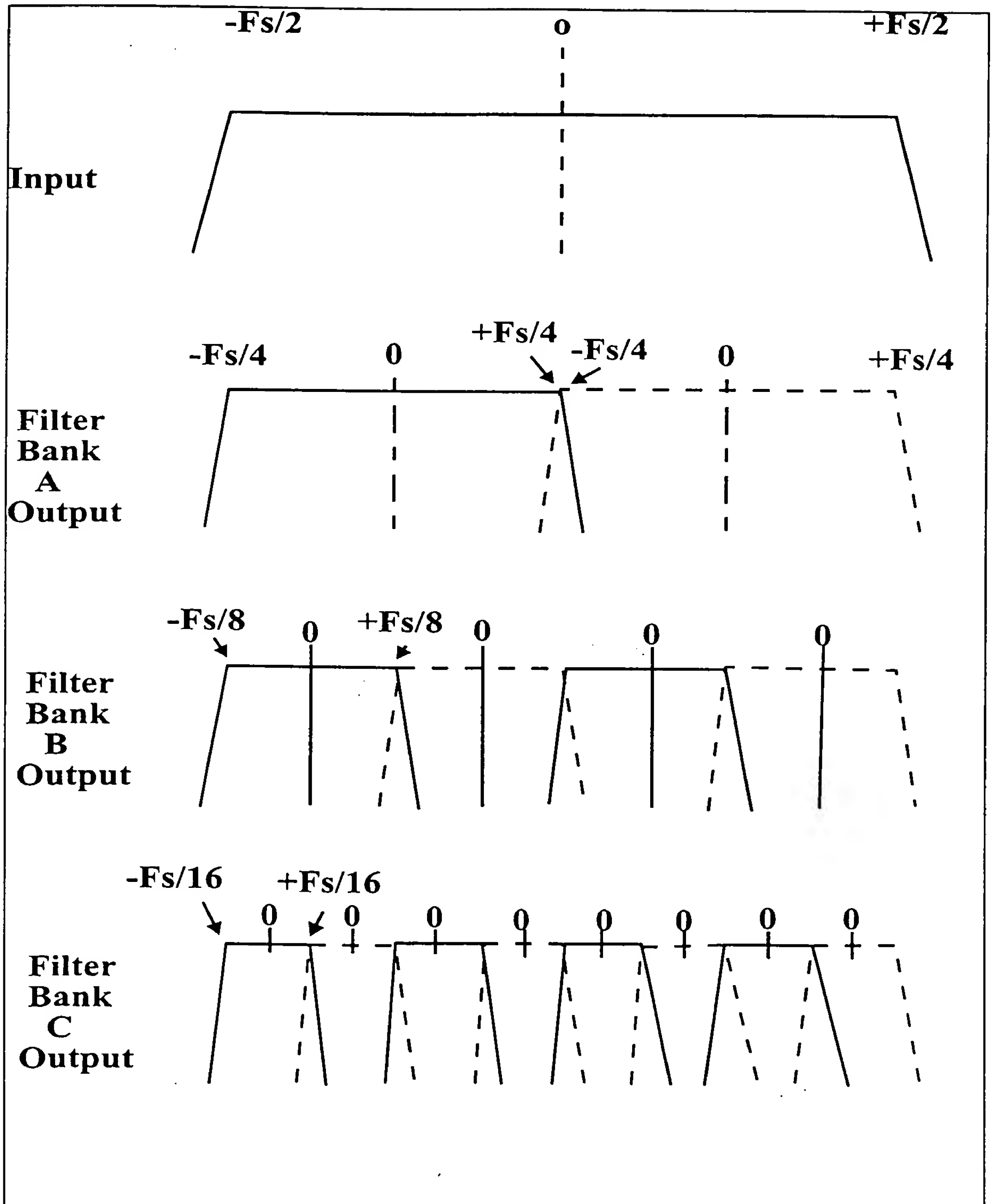

Fig. 2.2 Frequency Band Splitting

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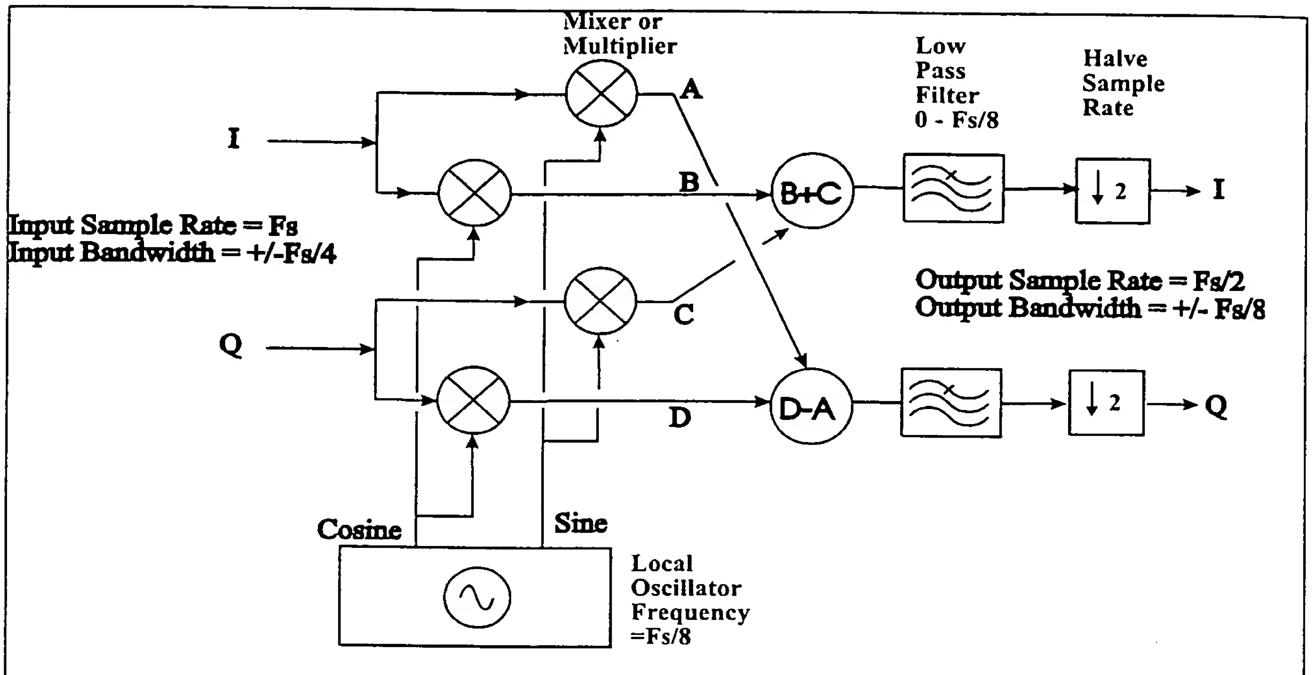

Fig. 2.3 Complex Down-Converter (CDC)

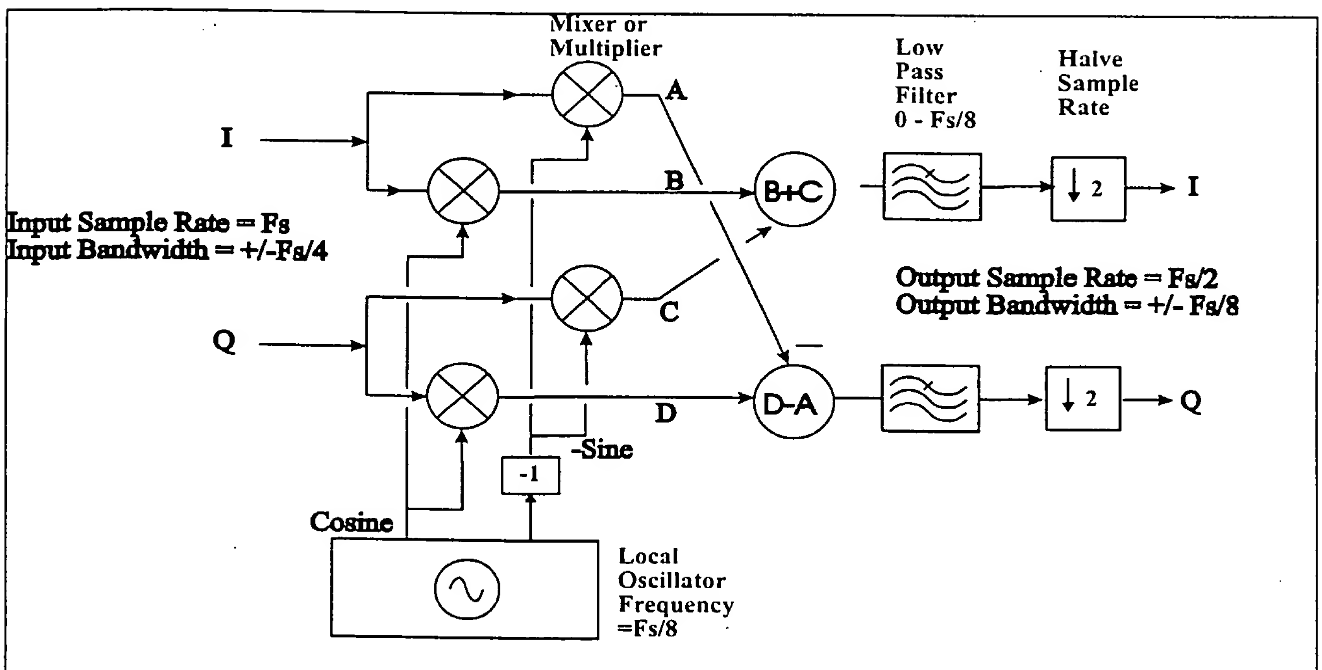

Fig. 2.4 Complex Up-Converter (CUC)

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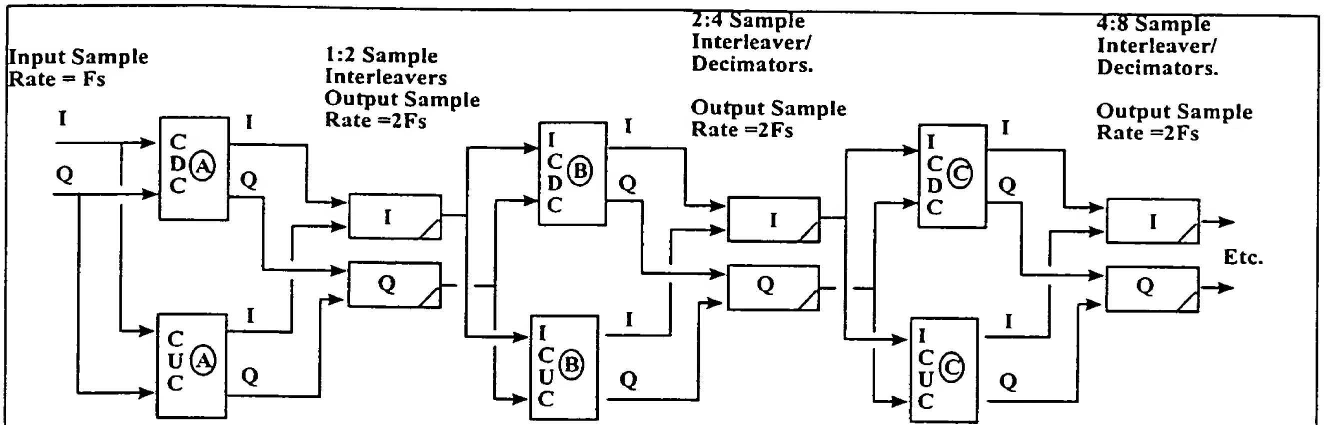

Figure 3.1 Block Diagram of Interleaved System

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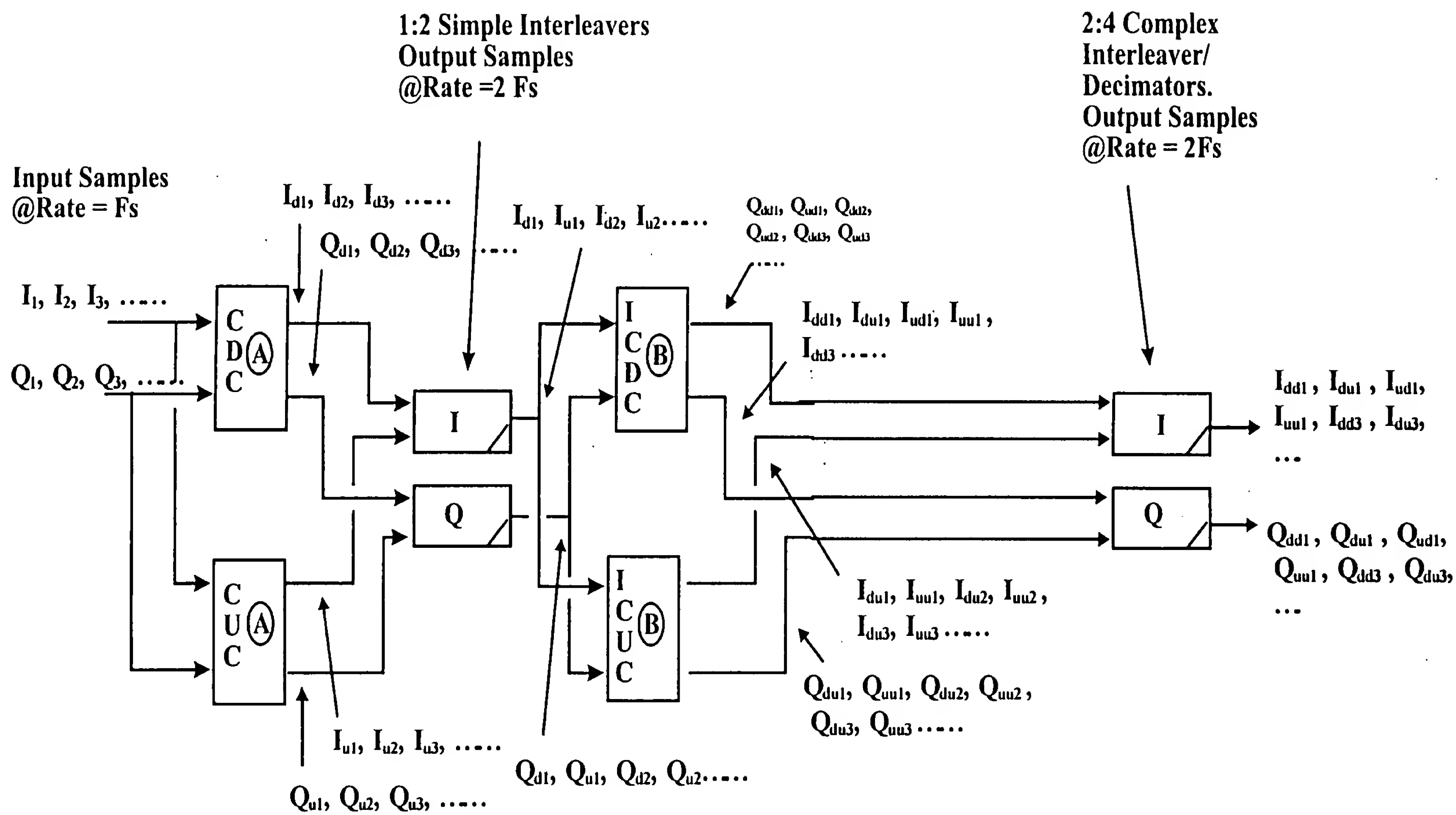

Figure 3.2 Detail of Interleavers